Application No.: 10/549,291

AMENDMENT TO CLAIMS

Please amend the claims as follows:

1. (Currently amended) A semiconductor device, comprising:

a semiconductor substrate in which a trench is formed, the semiconductor substrate contains an impurity of a first conductive type;

a source region and a drain region, each of which is buried in the trench and contains an impurity of ~~the same~~ a second conductive type;

a semiconductor FIN buried in part of the trench and provided between the source region and the drain region, the semiconductor FIN having an upper surface and both side surfaces;

a gate insulating film provided on the upper surface and the both side surfaces of the semiconductor FIN; [[and]]

a gate electrode formed directly on the gate insulating film and having a planar portion extending from the upper surface of the semiconductor FIN, over the upper portion of the trench, to portion of the semiconductor substrate in which the trench is not formed[[,]]; and

a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate,

wherein the gate electrode has in the trench, termination structures extending toward a bottom of the trench along the both sides of the semiconductor FIN.

2. (Original) The semiconductor device of claim 1, wherein the semiconductor FIN is made of one material selected from the group consisting of Si, $Si_{1-x}Ge_x$ ($0 < x \leq 1$), and $Si_{1-y-z}Ge_yC_z$ ($0 < y < 1$, $0 < z < 1$, $0 < y + z < 1$).

3. (Previously presented) The semiconductor device of claim 1, wherein an isolation insulating film is further provided between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode located over the side wall of the semiconductor FIN; and

wherein an insulating film is further provided between part of the semiconductor substrate in which the trench is not formed and the gate electrode.

4. (Previously presented) The semiconductor device of claim 1, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film is provided on part of the semiconductor substrate in which the trench is not formed as well as the both side surfaces and the upper surface of the semiconductor FIN, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode.

5. (Cancelled)

6. (Currently amended) A semiconductor device comprising:

a first field-effect transistor including a semiconductor substrate in which a trench is formed and containing an impurity of a first conductive type, a first source region and a first drain region each of which is buried in the trench and contains an impurity of ~~the same~~ a second

conductive type, a semiconductor FIN buried in part of the trench and provided between the first source region and the first drain region, the semiconductor FIN having an upper surface and both side surfaces, a first gate insulating film provided on the upper surface and the both side surfaces of the semiconductor FIN, and a first gate electrode formed directly on the first gate insulating film and having a planar portion extending from the upper surface of the semiconductor FIN, over the upper portion of the trench, to portion of the semiconductor substrate in which the trench is not formed, and a channel stopper formed in a region located at the bottom of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a higher concentration than that in the semiconductor substrate; and

a second field-effect transistor including a second gate insulating film provided on the semiconductor substrate, a second gate electrode provided on the second gate insulating film, and second source and drain regions each of which contains an impurity and is provided in a region of the semiconductor substrate located on a side of and under the second gate electrode,

wherein the first gate electrode having in the trench, termination structures extending from the upper surface of the semiconductor FIN toward a bottom of the trench along the both sides of the semiconductor FIN.

7. (Previously presented) The semiconductor device of claim 6, wherein the first field-effect transistor further includes an isolation insulating film formed between part of the semiconductor substrate located in a side wall portion of the trench and part of the first gate electrode provided over the side surface of the semiconductor FIN and a second insulating film formed between the semiconductor substrate in which the trench is not formed and the first gate electrode.

8. (Previously presented) The semiconductor device of claim 6, wherein the first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate,

wherein the first gate insulating film is provided on part of the semiconductor substrate in which the trench is not formed as well as the both side surfaces and the upper surface of the semiconductor FIN, and

wherein part of the first gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the first gate electrode.

9-11. (Canceled)

12. (Previously presented) The semiconductor device of claim 1, wherein the upper surface of the gate electrode has an even surface.

13. (Previously presented) The semiconductor device of claim 6, wherein the upper surface of the first gate electrode has an even surface.

14. (New) A semiconductor device comprising:

a semiconductor region of a conductive type having a main surface;

a trench formed in the semiconductor region and having a bottom portion;

a semiconductor FIN formed in the trench;

source and drain regions formed so as to be buried in the trench and connected to the

semiconductor FIN;

a gate insulating film formed so as to cover both side surfaces of the semiconductor FIN;

a gate electrode formed on the gate insulating film and having in the trench, termination structures extending toward the bottom portion of the trench along the both sides of the semiconductor FIN; and

a heavily doped impurity region of the conductive type formed in the semiconductor region at the bottom portion of the trench and under the semiconductor FIN and the source and drain regions.

15. (New) The semiconductor device of claim 14, wherein

the semiconductor device has a double-gate structure, and

a part of the gate insulating film formed above the semiconductor FIN has a larger thickness than a part of the gate insulating film formed in the side surfaces of the semiconductor FIN.

16. (New) The semiconductor device of claim 14, further comprising a first insulating film formed between the semiconductor FIN and the semiconductor region.

17. (New) The semiconductor device of claim 16, further comprising a second insulating film formed between the source and drain regions and the semiconductor region.

Application No.: 10/549,291

18. (New) The semiconductor device of claim 17, further comprising a third insulating film formed on the semiconductor region and the first insulating film, wherein the gate electrode is formed on the third insulating film.

19. (New) The semiconductor device of claim 14, wherein each width of the source and drain regions is larger than that of semiconductor FIN.

20. (New) The semiconductor device of claim 14, wherein the gate electrode does not entirely cover the side surfaces of the semiconductor FIN.

21. (New) The semiconductor device of claim 14, wherein a source-LDD region and a drain-LDD region are formed in the semiconductor FIN.

22. (New) The semiconductor device of claim 14, further comprising an insulating film formed between the semiconductor FIN and the semiconductor region and formed between the semiconductor region and the source and drain regions.